| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|---|---|---|---|---|---|
| 1 | BRS | L1 | 679 | (wafer or substrate) and (hard adj mask) and oxide and (photoresist or resist or resists or BARC) and (plasma adj3 etching) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2002/12/12 09:08 |
| 2 | BRS | L2 | 535 | 1 and (hole or holes or gap or gaps or aperture or apertures or trench or trenches) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2002/12/12 09:09 |
| 3 | BRS | L3 | 100699 | (oxide) adj10 (substrate or wafer) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2002/12/12 10:56 |
| 4 | BRS | L4 | 48418 | 3 same silicon | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2002/12/12 10:56 |
| 5 | BRS | L5 | 1430 | (pattern or patterning or patterned) adj10 (hard adj mask) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2002/12/12 10:57 |

| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|---|---|---|---|---|---|
| 6 | BRS | L6 | 4610 | (etch or etching or etched) adj10 silicon adj10 (gap or gaps or hole or holes or trench or trenches or aperture or apertures or via or vias) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2002/12/12 10:58 |
| 7 | BRS | L8 | 0 | (sacrificial adj layer) adj10 (hard adj mask) adj10 ((dry adj etch$3) or (plasma adj etch$3)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2002/12/12 11:00 |
| 8 | BRS | L7 | 127 | 5 and 6 | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2002/12/12 11:40 |
| 9 | BRS | L9 | 1430 | (pattern or patterning or patterned) adj10 (hard adj mask) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2002/12/12 11:41 |
| 10 | BRS | L10 | 84 | 9 same (plasma adj etching) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2002/12/12 11:41 |

| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|---|---|---|---|---|---|
| 11 | BRS | L11 | 16 | 10 same (resist or resists or BARC) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2002/12/12 11:52 |
| 12 | BRS | L12 | 48 | (trip or trips or stripping) adj10 (resist or resists or photoresist or photoresists) adj10 ((hard adj mask) or (silicon adj nitride) or (silicon adj oxynitride)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2002/12/12 11:54 |

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TITLE: Method for selecting from standardized set of integrated circuit mask features

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[0040] Yet another fabrication process that features self-aligned vias is described by Michael A. Corbett and John C. Davis in Solid State Technology magazine, October 2001, pp. 40-44. The following steps are used to fabricate vias and metal: deposit a dielectric layer, deposit a first hard mask layer, deposit a second hard mask layer, deposit photoresist, expose using the metal mask, develop, etch the second hard mask layer, strip photoresist, deposit photoresist, expose using the via mask, develop, etch the first hard mask layer, partially etch vias into the dielectric layer while simultaneously **stripping the photoresist, etch the first hard mask** layer thus transferring the metal pattern in the second hard mask layer to the first hard mask layer, etch trenches into the dielectric layer while simultaneously completing the etching of vias, strip the second hard mask layer, strip the first hard mask layer, fill vias and trenches with metal, and use chemical-mechanical polishing to remove excess metal and planarize the wafer. In this process, at least one hard mask layer separates the dielectric layer from photoresist, so that stripping photoresist cannot damage the dielectric layer. At the step where the first hard mask layer is first etched, vias are etched into the first hard mask layer only where specified by the via pattern in photoresist AND the metal

pattern in the second hard mask.